REMARKS

Claims 1-15 are pending. Claims 1-15 were rejected under 35 USC 112, second paragraph, as being indefinite. Claims 1-3, 9 and 10 were rejected under 35 USC 102(b) as being anticipated by Nakaya, US Patent No. 6,188,240. Claims 1, 14 and 15 were rejected under 35 USC 102(b) as being anticipated by New, US Patent No. 6,154,053. Claims 4-8 and 11-13 were indicated allowable if rewritten to overcome the rejections under 35 USC 112, second paragraph.

35 USC 112: Claims 1-15

The Examiner pointed out that claims 1 and 15 refer to "the K-LUT logic cell," which does not have a proper antecedent basis. The term "logic cell" has been deleted from claims 1, 3 and 15. Since no other basis was provided for rejecting claims 4-8 and 11-13, it is respectfully requested that such claims be allowed. Applicants thank the Examiner for his indication of allowable claims.

35 USC 102(b): Nakaya reference

The Examiner, citing Figure 17 of Nakaya, states on page 2 of the Office Action that Nakaya discloses independent claims 1 and 15. Applicants respectfully disagree, at least because claims 1 and 15 recite a "K input look-up table" with various features, and Figure 17 of Nakaya does not teach or suggest how individual look-up tables may be arranged or structured.

Figure 17 of Nakaya displays 3 programmable function blocks. Figure 3 illustrates one programmable function block containing a logic block, and Figure 5 uses multiplexers and logical gates to indicate how the logic block operates. See column 17, lines 5-7 in Nakaya.

The invention of Nakaya pertains to an improved logic circuit (see Abstract of Nakaya), whose inner workings are largely described using logical gates and multiplexers, as shown in Figure 5, rather than look-up tables. Look-up tables are data structures that may be the building blocks of logical gates and multiplexers. That is, a multiplexer, for example, may be made up of multiple look-up tables. The logic displayed in Figure 5, for example, may be made up of dozens if not hundreds of look-up tables.

In contrast to independent claims 1 and 15, Nakaya does not provide guidance on how individual look-up tables may be connected and arranged. Claims 1 and 15 refer to the inputs

and outputs of a K-input look up table. Nakaya does not indicate input or output lines connecting to a look-up table. Figure 5 of Nakaya instead shows input and output lines connecting to multiplexers 10.1-10.4, exclusive OR circuits 11.0-11.2, a NAND circuit 12, NOR circuit 13, NAND-OR circuit 14.0 and inverter 15.0. Applicants' attorney, using a word search, could find only one appearance of the term, "look-up table," in Nakaya and the term was not used to describe the invention, but instead to briefly summarize a feature of a conventional FPGA. See column 25, lines 35-37. In view of the foregoing, it is respectfully submitted that independent claims 1 and 15 are patentable over Nakaya.

35 USC 102(b): New reference

The Examiner, citing Figures 6-12 and 14-17, states on page 3 of the Office Action that New discloses independent claims 1 and 15. Applicants respectfully disagree for reasons similar to the ones presented above in connection with Nakaya.

New pertains to an arrangement involving configurable logic blocks (CLBs) and a carry logic circuit (See Abstract of New). Figure 14-17 are higher level diagrams including multiple connected blocks, where each block may represent a logic cell, function generator, carry logic block or other structures. Such logic cells may apparently be configured to perform the logic shown in Figures 6-12. See column 11, lines 62-65. Figures 6-12 illustrate such logic primarily through the use of multiplexers and logical gates.

In contrast to independent claims 1 and 15, however, New, like Nakaya, primarily shows arrangements of multiplexers and logical gates, rather than arrangements involving a look-up table. Claims 1 and 15 refer to the inputs and outputs of a K-input look up table. Nakaya does not indicate input or output lines connecting to a look-up table. As noted above, Figures 14-17 of Nakaya are higher level illustrations showing input and outputs connecting to functional blocks. Figures 6-12 show input and output lines extending from exclusive OR gates (e.g. OR gates 126-128 and 142-44 in Figure 6) and multiplexers (e.g. multiplexers 105-110 and 132-134 in Figure 6), but not from a look-up table. Applicants' attorney found only one instance of the term "look-up table" in New, where it is used to characterize function generator 121 in Figure 5. Figure 5 illustrates function generator 121 as being made of a 2-input, 1-output XOR gate. Such a structure clearly does not teach or suggest independent claims 1 and 15, which recite several additional features and limitations. In view of the foregoing, it is respectfully submitted that independent claims 1 and 15 are patentable over the prior art of record.

The various dependent claims are respectfully submitted to be patentable over the art of record for at least the same reasons as set forth above with respect to their associated

independent claims. Furthermore, these dependent claims recite additional features that when considered in the context of the claimed invention, further patentably distinguish the art of record.

The Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution, Applicant's attorney, Eric Yoon, can be reached at the telephone number set out below. If any additional fees are due in connection with the filing of this amendment, the Commissioner is authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP196.)

Respectfully submitted,
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